What is claimed is:

1. A correlator for correlating an input signal with a code, comprising:

a sample register adapted to store and output E input samples every chip period of an input sample stream clocked at an over sampling ratio of R times a nominal sampling clock rate;

a code register adapted to store and output a code value at said nominal sampling clock rate;

a multiplier coupled to said sample register and said code register, said multiplier adapted to multiply the output of said sample register with the output of said code register;

an adder adapted to add the output of said multiplier with the correlation sum output of the last stage of an M-stage integration result shift register and to produce a correlation sum therefrom;

said integration results shift register adapted to store M correlation sums wherein correlation sums output of said adder are shifted into said integration results shift register at said over sampling clock rate such that the over sampling phase of the correlation sum at the output of said integration results shift register corresponds to the correlation sum currently at the input to said adder; and

wherein E, R and M are positive integers.

2. The correlator according to claim 1, wherein said code register is adapted to be loaded with a new code value once every R over sampling cycles.

3. The correlator according to claim 1, wherein said code register is loaded with code values output by a code generator.

4. The correlator according to claim 1, wherein said sample register, said code register, said multiplier, said adder and said integration result shift register are adapted to process and output complex values.

5. The correlator according to claim 1, wherein the effective over sampling ratio E is equal to the number of shift register stages M.

6. A correlator for correlating input samples with a plurality of codes, comprising:

a sample register adapted to store and output input samples at a first clock rate;

an N-stage circular code shift register adapted to store N code values and clocked at a second clock rate;

a multiplier coupled to said sample register and said code shift register, said multiplier for multiplying input samples with the code value output of the last stage of said code shift register, wherein said code shift register is circularly shifted such that each input sample is sequentially multiplied by each of N codes;

an adder adapted to add the output of said multiplier with the correlation sum output of the last stage of an M-stage integration result shift register and to produce a correlation sum therefrom;

said integration results shift register adapted to store M correlation sums wherein correlation sums output of said adder are shifted into said integration results shift register at said second clock rate such that the correlation sum at the output of said integration results shift register corresponds to that of the correlation sum currently at the input to said adder; and

wherein N and M are positive integers.

7. The correlator according to claim 6, wherein said second clock rate is equal to N times said first clock rate.

8. The correlator according to claim 6, wherein said first clock rate is equal to a nominal sampling rate and wherein the number of integration result shift register stages M is equal to the number of code shift register stages N.

9. The correlator according to claim 6, wherein said first clock rate is equal to an over sampling rate R times a nominal sampling rate and wherein the number of integration result shift register stages M is equal to the number of code shift register stages N times R, wherein R is a positive integer.

10. The correlator according to claim 6, wherein said sample shift register, said code shift register, said multiplier, said adder and said integration result shift register are adapted to process and output complex values.

11. The correlator according to claim 6, wherein said code shift register is adapted to be parallel loaded with N code values once every input sample interval.

12. The correlator according to claim 6, wherein said code shift register is adapted to be parallel loaded with N code values once every R over sampling intervals, wherein R is a positive integer.

13. The correlator according to claims 11 or 12, wherein said N code values are provided by a code generator.

14. The correlator according to claim 6, wherein said integration result shift register comprises T registers and selection means arranged such that a one or more of said T registers are selectably configured in accordance with a length selection signal to receive and store correlation sums output from said adder and to function as a shift register unit, and wherein T is a positive integer.

15. The correlator according to claim 14, wherein said selection means comprises T-1 multiplexers located between each integration result register and configured to output either the output of said adder or the output of the integration result register adjacent thereto in accordance with said length selection signal.

16. A rake receiver for use in a Code Division Multiple Access (CDMA) spread spectrum communications system, comprising:

a radio frequency (RF) front end circuit for receiving a spread spectrum RF signal having a plurality of multipath components;

a searcher adapted to measure the multipath components of said RF signal and to generate one or more path selections in accordance thereto;

a collapsed finger bank for generating a plurality of demodulated signals from said RF signal in accordance with said path selections, said collapsed finger bank comprising:

a sample register adapted to store and output input samples at a first clock rate;

an N-stage circular code shift register adapted to store N code values and clocked at a second clock rate;

a multiplier coupled to said sample register and said code shift register, said multiplier for multiplying input samples with the code value output of the last stage of said code shift register, wherein said code shift register is circularly shifted such that each input sample is sequentially multiplied by each of N codes;

an adder adapted to add the output of said multiplier with the correlation sum output of the last stage of an M-stage integration result shift register and to produce a correlation sum therefrom;

said integration results shift register adapted to store M correlation sums wherein correlation sums output of said adder are shifted into said integration results shift register at said second clock rate such that the correlation sum at the output of said integration results shift register corresponds to that of the correlation sum currently at the input to said adder;

a results register adapted to store final correlation sums output of said integration results register and to output said final correlation sums as demodulated signals;

wherein N and M are positive integers;

a channel estimation unit adapted to generate channel estimates of one or more pilot signals; and

a combiner coupled to the output of said collapsed finger bank and adapted to combine said demodulated signals output therefrom to generate a receive data output signal in accordance with said channel estimates.

17. The receiver according to claim 16, further comprising a channel decoder adapted to decode said receive data output signal and to generate a decoded output signal therefrom.

18. The correlator according to claims 1 or 6, further comprising a result register coupled to the output of the last stage of said integration results shift register and adapted to sequentially store final correlation sums output therefrom.

19. The device according to claims 1, 6 or 16, further comprising timing means adapted to provide suitable timing, control and clock signals to said correlator.

20. The device according to claims 1, 6 or 16, further comprising means for zeroing out each individual correlation sum when integration thereof is complete.

21. The device according to claims 1, 6 or 16, wherein said zeroing means comprises a multiplexer adapted to select either the output of the last stage of said integration results shift register or a zero value in accordance with a result enable signal, wherein said result enable signal is active only when integration is complete.

22. The device according to claims 1, 6 or 16, further comprising counting means for determining when integration is complete for each correlation sum in accordance with a spreading factor input to said counting means.

23. The device according to claims 1, 6 or 16, further comprising means for simultaneously outputting and storing a final correlation sum sequentially in a results register and zeroing out each individual correlation sum when integration thereof is complete.

24. The device according to claims 1, 6 or 16, wherein said multiplier is adapted to multiply hard-limited 1-bit versions of said input signal.

25. The device according to claims 1, 6 or 16, wherein said code values are provided by a code generator adapted to output a non-binary code.

26. The device according to claims 1, 6 or 16, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

27. The device according to claims 1, 6 or 16, adapted to be implemented in a Field Programmable Gate Array (FPGA).

28. A method of correlating a first plurality of input samples with a second plurality of codes, said method comprising the steps of:

receiving and storing input samples in an input sample register at a first clock rate;

receiving and storing N code values in a circular code shift register and outputting said code values at a second clock rate;

multiplying said input samples with the code value output of the last stage of said code shift register to generate multiplication results, wherein said code shift register is circularly shifted such that each input sample is sequentially multiplied by each of N codes;

adding each multiplication result to its corresponding correlation sum;

storing M correlation sums in an M-stage integration result shift register and shifting said wherein correlation sums output of said adder into said integration results shift register at said second clock rate such that the correlation sum at the output of said integration results shift register corresponds to that of the correlation sum currently being added; and

wherein N and M are positive integers.

29. The method according to claim 24, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

30. The method according to claim 24, adapted to be implemented in a Field Programmable Gate Array (FPGA).

31. A multiply and accumulate (MAC) apparatus for multiplying two signals and accumulating the results thereof, comprising:

input storage means adapted to store and output first input samples;

second storage means adapted to store and circularly rotate a plurality of second input samples;

multiplier means coupled to said first storage means and said second storage means and adapted to multiply the output of said input storage means by the output of said second storage means, wherein said second storage means is circularly rotated such that each first input sample is sequentially multiplied with said plurality of second input samples;

result storage means adapted to simultaneously store and output one or more MAC results in a first-in first-out manner;

summing means adapted to add the output of said multiplier means with the MAC result output of said result storage means to produce an updated MAC result therefrom, said updated MAC result input to said result storeage means; and

wherein said second storage means and said result storage means are adapted such that the MAC product from said multiplier means present at a first input to said summing means corresponds to the MAC result output from said result storage means present at a second input to said summing means.

32. The device according to claims 31, wherein said multiplier means is adapted to multiply hard-limited 1-bit versions of said first input signals and said second input samples.

33. The apparatus according to claim 31, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

34. The apparatus according to claim 31, adapted to be implemented in a Field Programmable Gate Array (FPGA).